UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,493	09/27/2001	Arthur Allan Bayot	TI-33474 (032350.B352)	8827

23494 7590 02/14/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/963,493
Filing Date: September 27, 2001
Appellant(s): BAYOT, ARTHUR ALLAN

W. Daniel Swayze, Jr. 34,478
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 24, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-6 and 12-16 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

For the above reasons, it is believed that the rejections should be sustained.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,059,172	Chapman et al.	05-2000
5,205,032	Kuroda et al.	04-1993

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Chapman et al., U.S. Patent 6,059,172.

3. Chapman discloses a semiconductor process as claimed. See **FIGS. 1-5**, where Chapman teaches a method of manufacturing a ball grid array semiconductor package comprising the steps of:

providing a substrate **10**, wherein said substrate comprises a first surface and a second surface and said first surface or said second surface comprises a conductor pattern;

providing a plurality of conductive bump contact areas **9** on said first surface of said substrate;

substantially aligning each of said conductive bump contact areas with at least one conductive bump **6**, wherein the step of substantially aligning said conductive bump contact areas with at least one of said conductive bumps comprises the step of vibrating at least a portion

of said substrate, wherein said vibration of at least a portion of said substrate substantially aligns each of said conductive bump contact areas with at least one of said conductive bumps; and

disposing at least one of said conductor bumps on each of said conductive bump contact areas (column 2, lines 24-39).

Pertaining to claim 12, Chapman discloses a method of manufacturing a ball grid array semiconductor package comprising the steps of:

providing a substrate 10 wherein said substrate comprises a first surface and a second surface and said first surface or said second surface comprises a conductive pattern;

providing a plurality of conductive bump contact areas 9 on said first surface of said substrate;

substantially aligning each of said conductive bump contact areas with at least one conductive bump, wherein the step of substantially aligning said conductive bump contact areas with at least one of said substrate, wherein said vibration of at least a portion of said substrate substantially aligns each of said conductive bump contact areas with at least one of said conductive bumps;

disposing at least one of said conductive bumps on each of said conductive bump contact areas; and

reflowing said conductive bump disposed on said conductive bump contact areas (see column 2, lines1-4 for the reflow step).

Claim Rejections - 35 USC § 103

4. Claims 2, 3, 4,5, 13, 14, 15 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman et al., U.S. Patent 6,059,172 as applied to claim 1 above, and further in view of Kuroda et al., U.S. Patent 5,205,032.

5. Pertaining to claims 2 and 13, Chapman fails to teach the method of claims 1 and 12, wherein the step of vibrating at least a portion of said substrate comprises the step of ultrasonically vibrating at least a portion of said substrate. Kuroda teaches wherein the vibration comprises ultrasonic vibration. In view of Kuroda, it would have been obvious to one of ordinary skill in the art to incorporate ultrasonic vibration into the Chapman semiconductor process because ultrasonic vibration is a comprises a electromagnetic vibrating element (column 3, lines 65-68).

6. Pertaining to claims 3 and 14, Chapman in view of Kuroda teaches the method of claims 2 and 12, wherein the step of ultrasonically vibrating at least a portion of

said substrate comprises the step of ultrasonically vibrating a first end, a second end, and a third end of a film strip on which at least one of said substrates is disposed. In view of Kuroda, it would have been obvious to one of ordinary skill in the art to incorporate ultrasonic vibration into the Chapman semiconductor process because ultrasonic vibration is a comprises a electromagnetic vibrating element (column 3, lines 65-68).

7. Pertaining to claims 4 and 15, Chapman in view of Kuroda teaches the method of claims 2 and 12, further comprising the step of discontinuing said ultrasonic vibration of at least a portion of said substrate when each of said conductive bump contact areas are substantially

aligned with at least one of said conductive bumps. In view of Kuroda, it would have been obvious to one of ordinary skill in the art to incorporate ultrasonic vibration into the Chapman semiconductor process because ultrasonic vibration is a comprises a electromagnetic vibrating element (column 3, lines 65-68).

8. Pertaining to claims 5 and 16, Chapman in view of Kuroda teaches the method of claims 4 and 12, wherein said conductive bumps comprise solder.

(11) Response to Argument

Appellant arguments filed August 18, 2003 have been fully considered but they are not persuasive.

Appellant contends that the 35 U.S.C. 102(b) rejection of claim 1 is improper because Applicants contend that term "vibrating at least a portion of the substrate" is not disclosed by Chapman, et el., U.S. Patent 6,059,172 herein known as Chapman.

In response to Appellant contention that Chapman fails disclose "vibrating", attention is are directed to column 2, lines 24-29 where Chapman clearly discloses a method of substantially aligning conductive bump contact areas with at least one conductive bump using a vibration method. Please note that Chapman clearly states that vibration, brushing and vacuum, in association with an alignment plate have been proposed for dealing with solder balls. Since the limitation is recited in the reference, Chapman meets Applicants claimed limitation.

Application/Control Number: 09/963,493
Art Unit: 2823

Conferees

OC

Olik Chaudhuri, Supervisory Primary Examiner

W.F

Wael Fahmy, Supervisory Primary Examiner

W. David Coleman, Primary Examiner

W. DAVID COLEMAN
PRIMARY EXAMINER